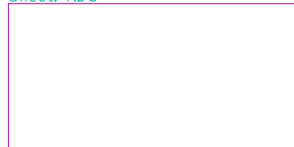


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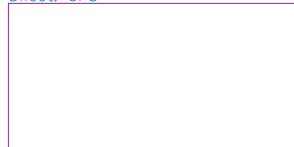
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Sheet: FPGA\_Power



File: kiwi.FPGA\_power.sch

Sheet: GPS



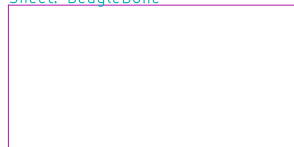
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Sheet: Power\_Supplies



File: kiwi.power\_supplies.sch

Sheet: BeagleBone



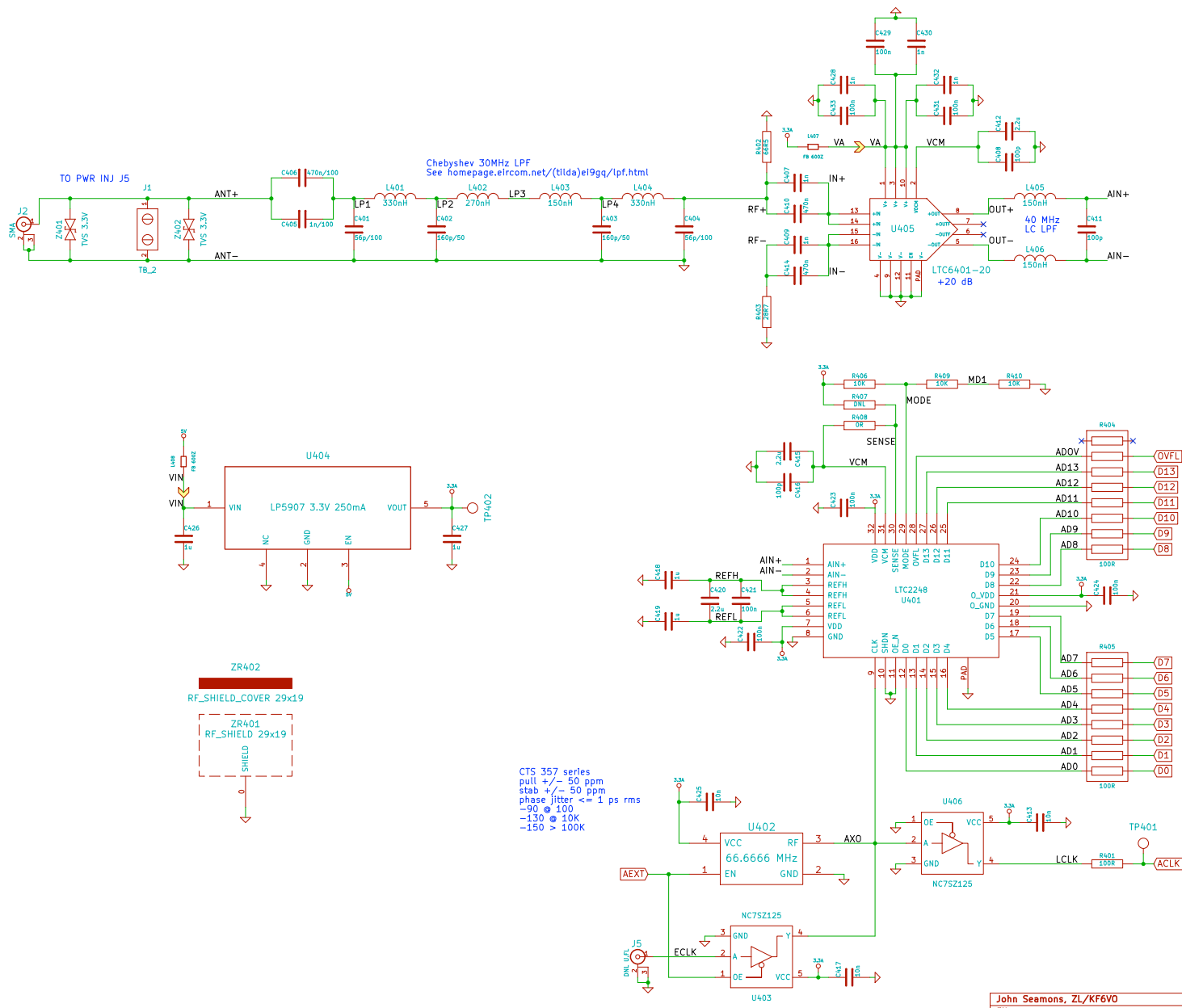
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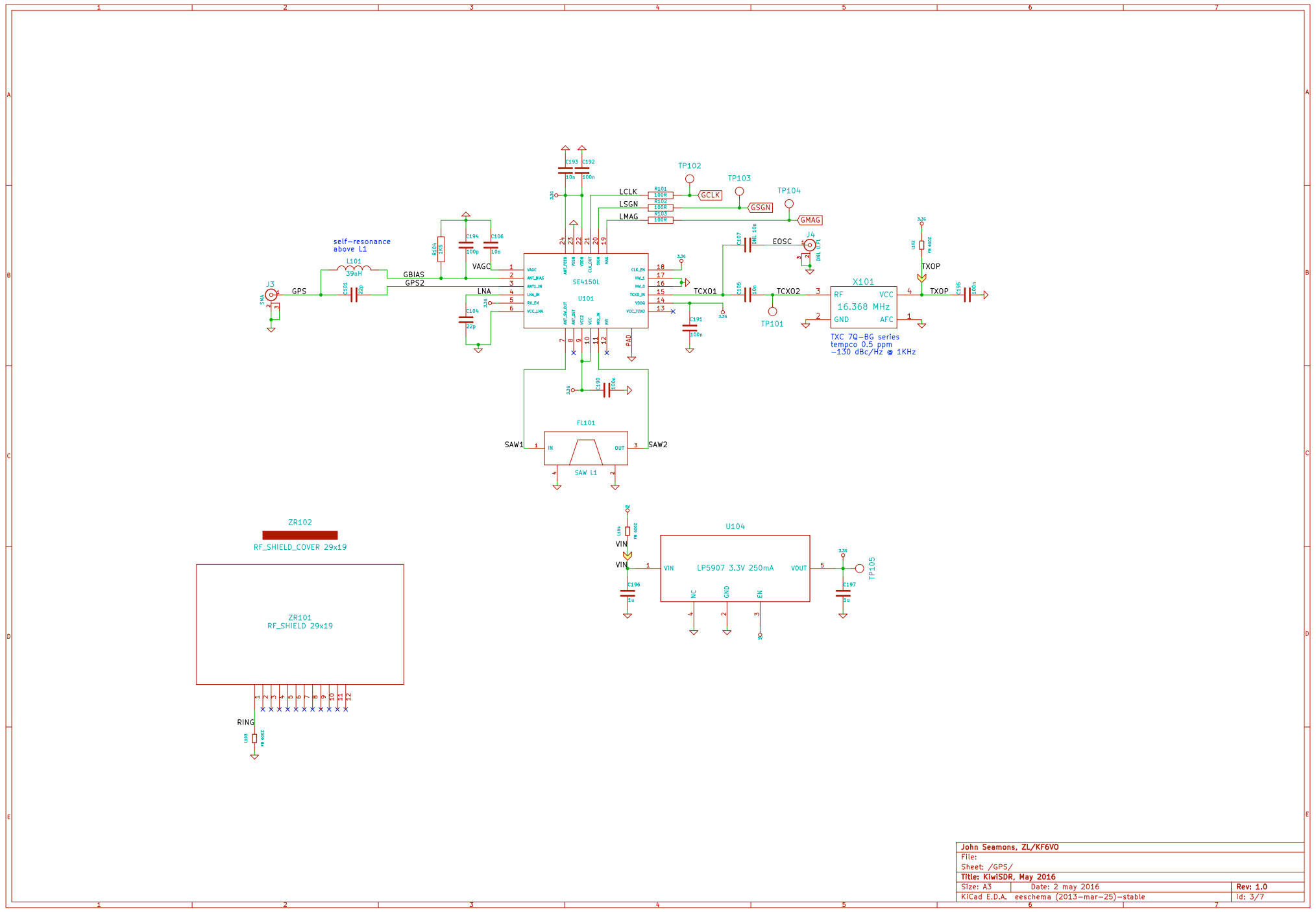
Sheet: FPGA\_IO

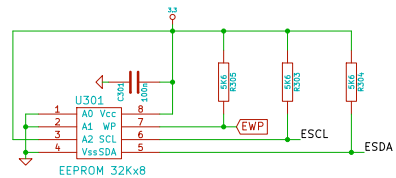
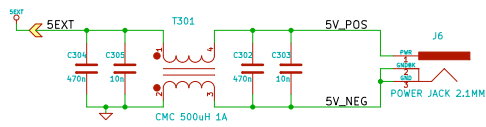
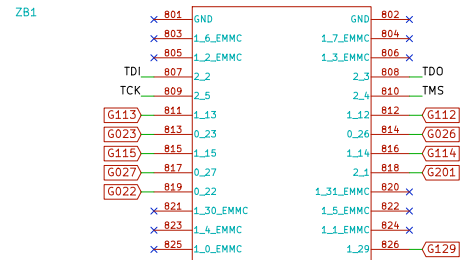
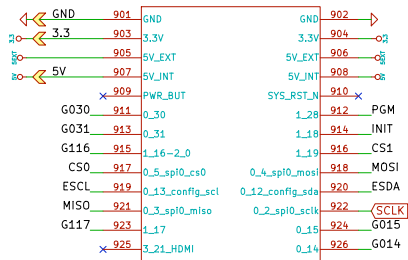
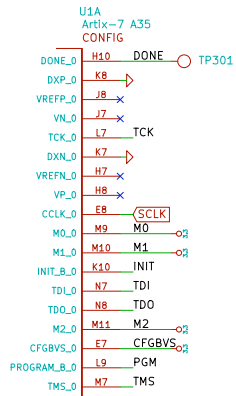
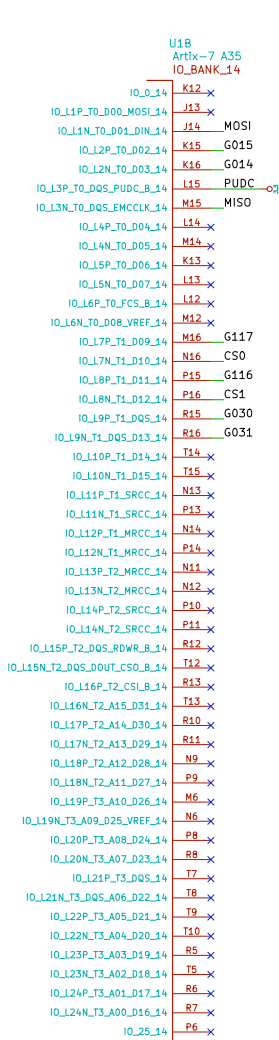


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File:		
Sheet: /		
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U1D  
Artix-7 A35  
IO\_BANK\_34

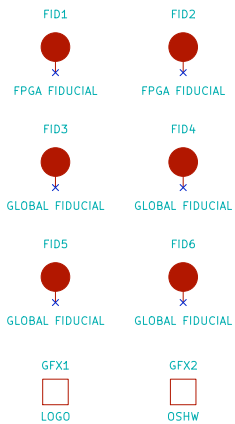
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IO\_13P\_TO\_DQS\_34 N3 G023  
IO\_13N\_TO\_DQS\_34 N2 G115  
IO\_14P\_TO\_34 N1 G114  
IO\_14N\_TO\_34 P1 G026  
IO\_15P\_TO\_34 P4 X  
IO\_15N\_TO\_34 P3 X  
IO\_16P\_TO\_34 M5 X  
IO\_16N\_TO\_VREF\_34 N4 X  
IO\_17P\_T1\_34 R2 G112  
IO\_17N\_T1\_34 R1 G113  
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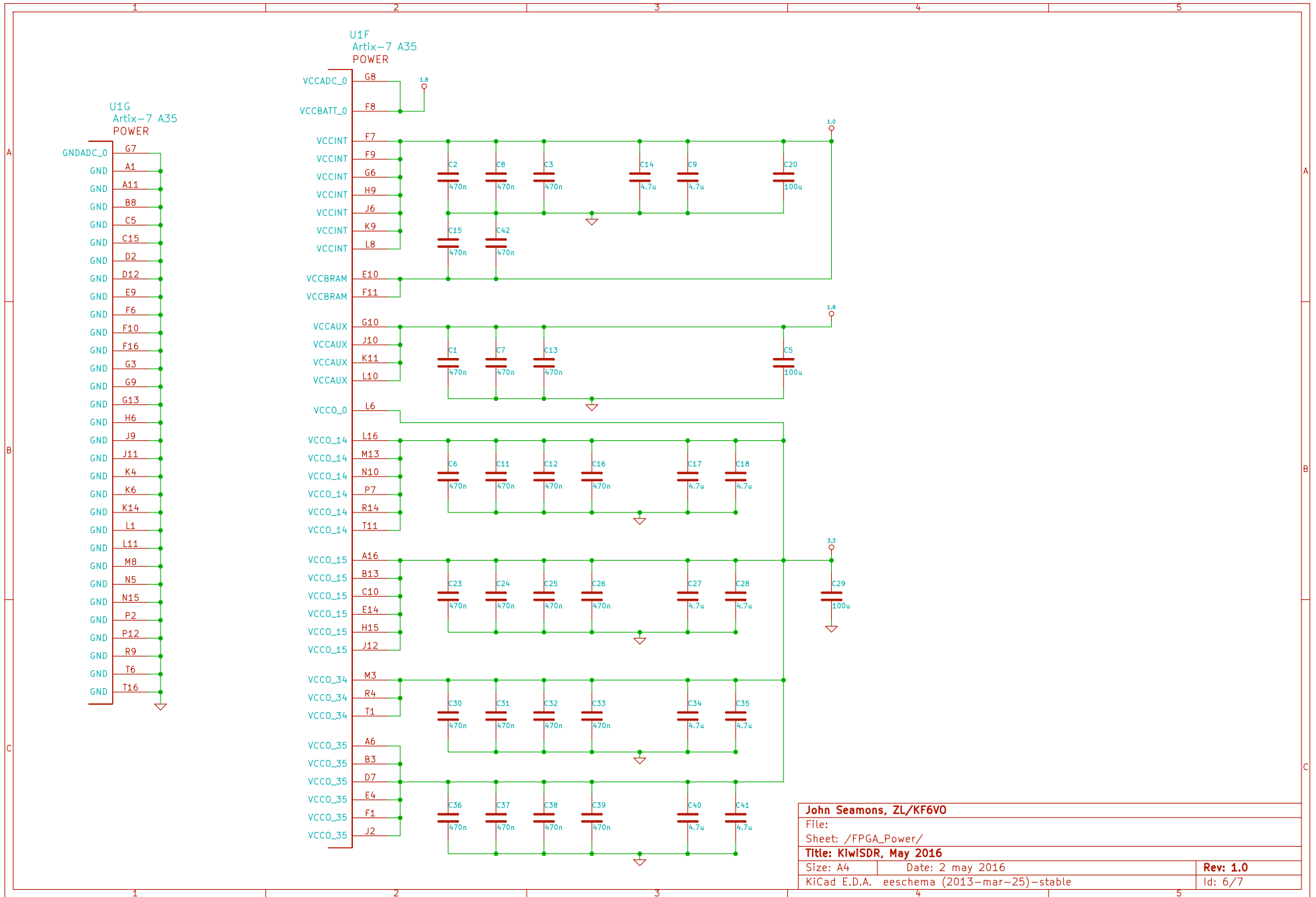
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IO\_14N\_TO\_35 A3 X  
IO\_15P\_TO\_AD13P\_35 C7 X  
IO\_15N\_TO\_AD13N\_35 C6 X  
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IO\_18P\_T1\_AD14P\_35 B2 GMAG  
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IO\_141N\_T1\_SRCC\_35 D3 X  
IO\_142P\_T1\_MRCC\_35 D4 GCLK  
IO\_142N\_T1\_MRCC\_35 C4 X  
IO\_143P\_T2\_MRCC\_35 F5 X  
IO\_143N\_T2\_MRCC\_35 E5 X  
IO\_144P\_T2\_SRCC\_35 F4 X  
IO\_144N\_T2\_SRCC\_35 F3 X  
IO\_145P\_T2\_DQS\_35 F2 X  
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IO\_146P\_T2\_35 G5 X  
IO\_146N\_T2\_35 G4 X  
IO\_147P\_T2\_35 G2 X  
IO\_147N\_T2\_35 G1 X  
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IO\_149P\_T3\_35 J5 X  
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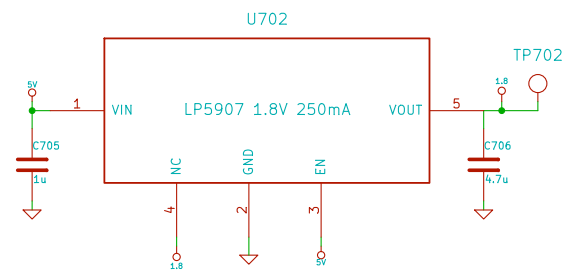
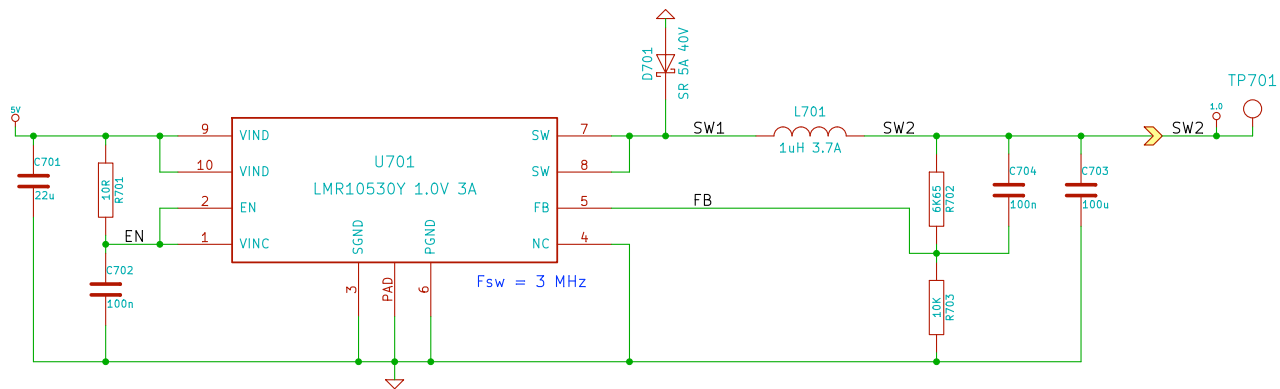
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IO\_146N\_T2\_A27\_15 F13 X  
IO\_147P\_T2\_A26\_15 E16 D13  
IO\_147N\_T2\_A25\_15 D16 D14  
IO\_148P\_T2\_A24\_15 F15 OVFL  
IO\_148N\_T2\_A23\_15 E15 D12  
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